RT6321AN-A, 23V_{IN}, 12A Buck Converter Evaluation Board

General Description

The Evaluation Board demonstrates the RT6321AN-A to be designed for a programmed between 0.6V to 5.5V/12A output from a 4.5V to 23V input at 500kHz switching frequency. The RT6321AN-A provides complete protection functions such as input undervoltage-lockout, output undervoltage protection, overcurrent protection and thermal shut down. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up.

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Performance Specification Summary

Summary of the RT6321AN-A Evaluation Board performance specificiaiton is provided in Table 1. The ambient temperature is 25°C.

Table 1. RT6321AN-A Evaluation Board Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range		4.5	--	23	V
Output Current		0	--	12	A
Default Output Voltage		--	1.05	--	V
Operation Frequency		--	500	--	kHz
Output Ripple Voltage	I_{OUT} = 12A	--	22	--	mVp-p
Line Regulation	I_{OUT} = 12A, V_{IN} = 4.5V to 23V	--	±1	--	%
Load Regulation	V_{IN} = 12V, I_{OUT} = 0.001A to 12A	--	±1	--	%
Load Transient Response	V_{OUT} = 1.05V , I_{OUT} = 1.2A to 12A	--	±5	--	%
Maximum Efficiency	V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 2A, VCC_EXT = 5V	--	91	--	%

Power-up Procedure

Suggestion Required Equipments

- RT6321AN-A Evaluation Board
- DC power supply capable of at least 25V and 6A
- Electronic load capable of 12A
- Function Generator
- Oscilloscope

Quick Start Procedures

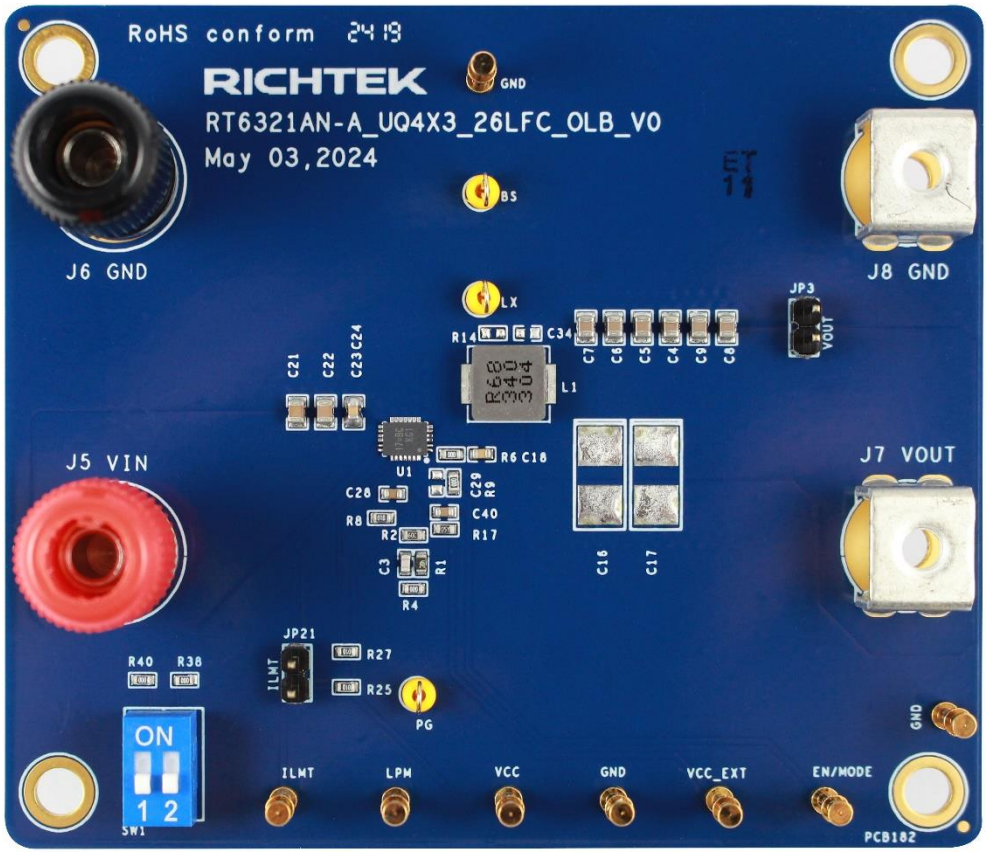
The Evaluation Board is fully assembled and tested. Follow the steps below to verify board operation. Do not turn on supplies until all connections are made. When measuring the output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the output voltage ripple by touching the probe tip and ground ring directly across the last output capacitor.

Proper measurement equipment setup and follow the procedure below.

1) With power off, connect the input power supply to the VIN and GND pins.
2) With power off, connect the electronic load between the VOUT and nearest GND pins.
3) Turn on the power supply at the input. Make sure that the input voltage does not exceeds 23V on the Evaluation Board.
4) Check for the proper output voltage using a voltmeter.
5) Once the proper output voltage is established, adjust the load within the operating ranges and observe the output voltage regulation, ripple voltage, efficiency and other performance.

Detailed Description of Hardware

Headers Description and Placement



Carefully inspect all the components used in the EVB according to the following Bill of Materials table, and then make sure all the components are undamaged and correctly installed. If there is any missing or damaged component, which may occur during transportation, please contact our distributors or e-mail us at evb_service@richtek.com.

Test Points

The EVB is provided with the test points and pin names listed in the table below.

Test Point/ Pin Name	Function
VIN	Input voltage.
VOUT	Output voltage.
GND	Ground.
EN/MODE	Enable and operation mode control input.
VCC_EXT	External voltage input for VCC.
VCC	Internal LDO output. Used as supply to internal control circuits. DO NOT connect to any external loads.

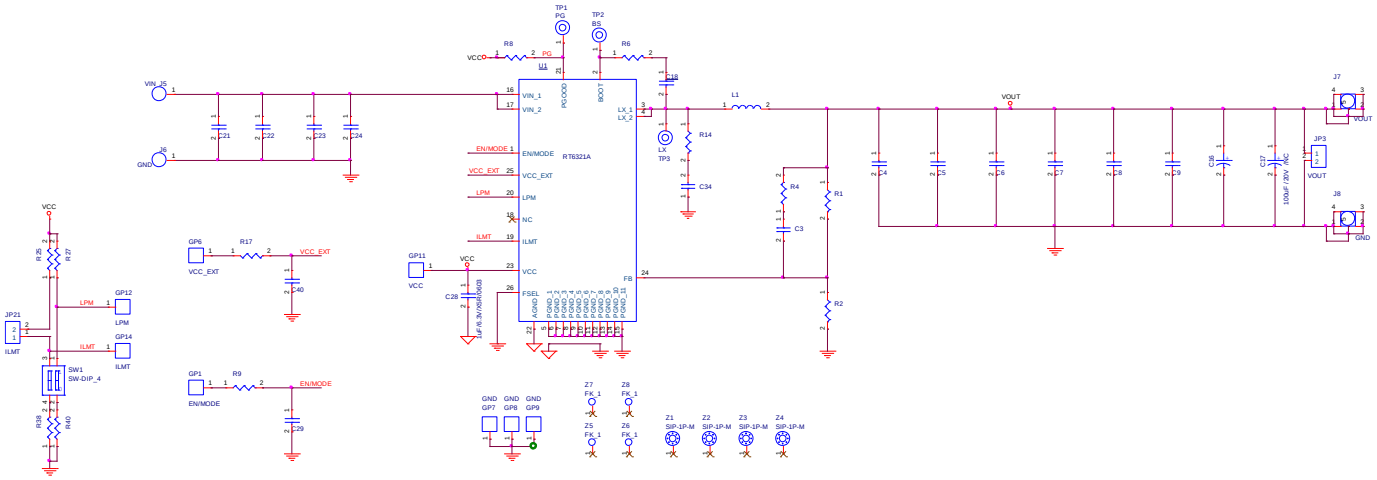
Test Point/ Pin Name	Function
LPM	Low power mode control input pin.
ILMT	Valley current-limit setting pin. 14A: Connect the ILMT pin to PGND. 16A: Leave the ILMT pin floating/open. 18A: Connect the ILMT pin to 5V.
JP21	ILMT jumper. Connect ILMT to VCC or floating.
LX	Switch node test point.
PG	Power good indicator.
BS	Bootstrap test pin.
JP3	VOUT ripple measure test pin.

Bill of Materials

V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 12A, f_{SW} = 500kHz						
Reference	Count	Part Number	Value	Description	Package	Manufacturer
U1	1	RT6321A	RT6321AN-A	Buck Converter	UQFN-26L 4x3 (FC)	RICHTEK
C3	1	0603N680J500CT	68pF	Capacitor, Ceramic, 50V, NPO	0603	WALSN
C4, C5, C6, C7, C8, C9	6	0805X226M6R3CT	22µF	Capacitor, Ceramic, 6.3V, X5R	0805	WALSN
C18, C24	2	0603B104K500CT	0.1µF	Capacitor, Ceramic, 50V, X7R	0603	WALSN
C21, C22	2	0805X106K250CT	10µF	Capacitor, Ceramic, 25V, X5R	0805	WALSN
C28	1	0603X475K6R3CT	4.7µF	Capacitor, Ceramic, 6.3V, X5R	0603	WALSN
C40	1	0603X475K6R3CT	4.7µF	Capacitor, Ceramic, 6.3V, X5R	0603	WALSN
L1	1	PEUE063T-R68MS	0.68µH	Inductor, Isat = 18.5A, 4.3mΩ	7.3x6.8x3mm	CYNTEC
R1	1	RTT033092FTP	30.9k	Resistor, Chip, 1/10W, 1%	0603	RALEC
R2	1	WR06X4122FTL	41.2k	Resistor, Chip, 1/10W, 1%	0603	WALSIN
R4, R6, R9, R38, R40	5	WR06X000 PTL	0	Resistor, Chip, 1/10W, 1%	0603	WALSIN
R8, R25, R27	3	WR06X1003FTL	100k	Resistor, Chip, 1/10W, 1%	0603	WALSIN
R17	1	WR06W1R10FTL	1.1	Resistor, Chip, 1/10W, 1%	0603	WALSIN

Typical Applications

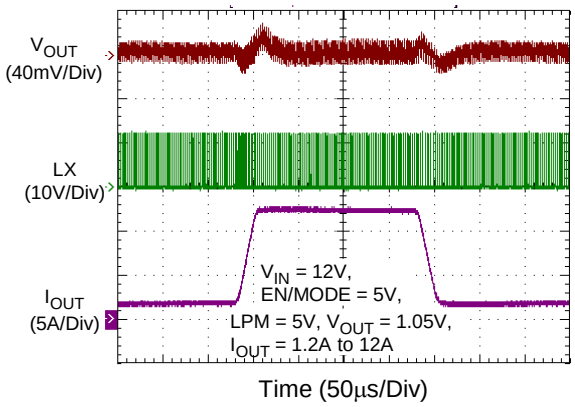
EVB Schematic Diagram



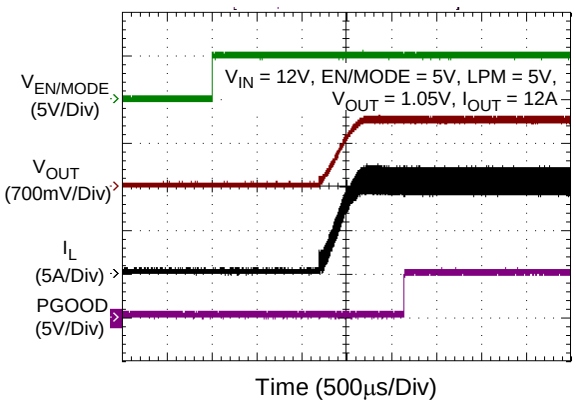
1. The capacitance values of the input and output capacitors will influence the input and output voltage ripple.
2. MLCC capacitors have degrading capacitance at DC bias voltage, and especially smaller size MLCC capacitors will have much lower capacitance.

Measure Result

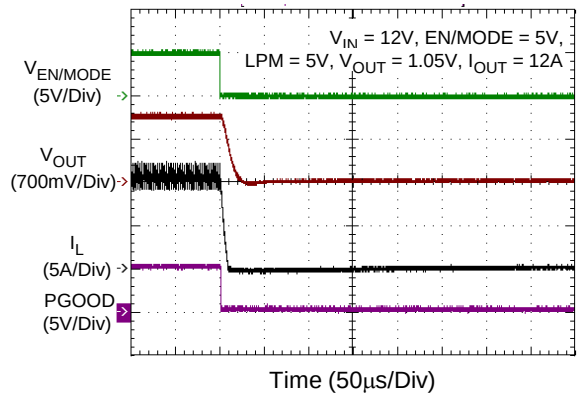
Load Transient Response



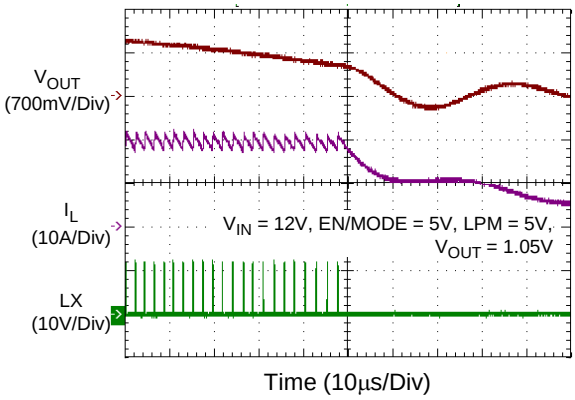
Power On from EN/MODE



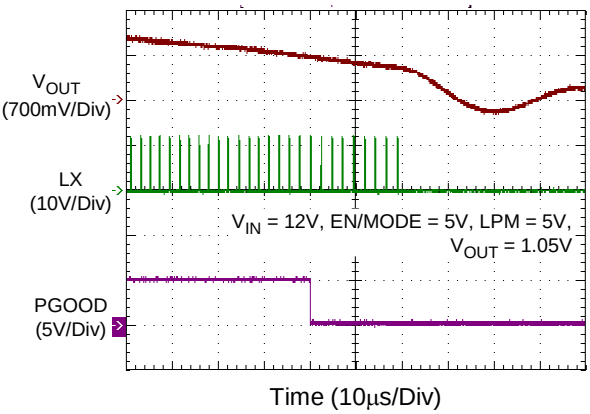
Power Off from EN



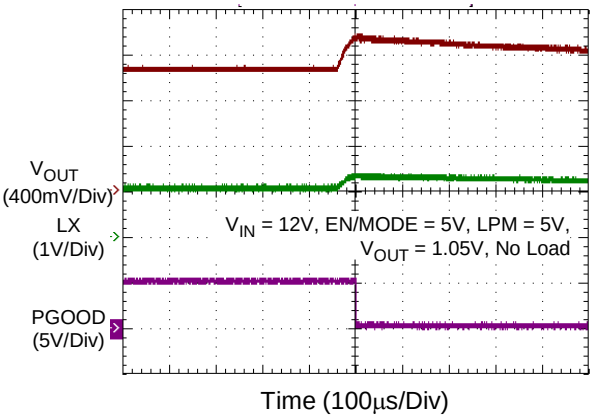
Overcurrent Limit



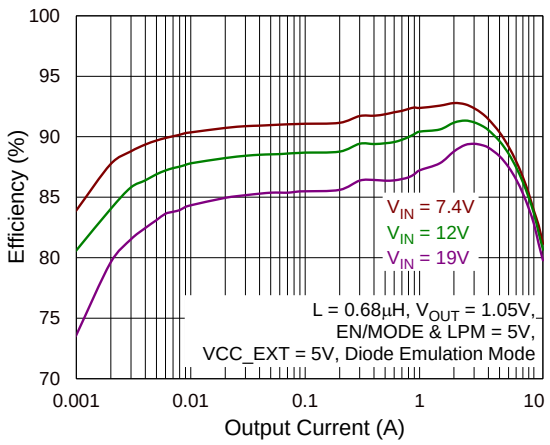
VOUT UVP



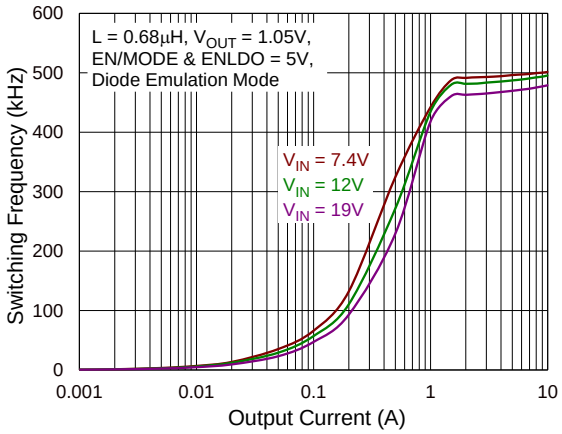
VOUT OVP



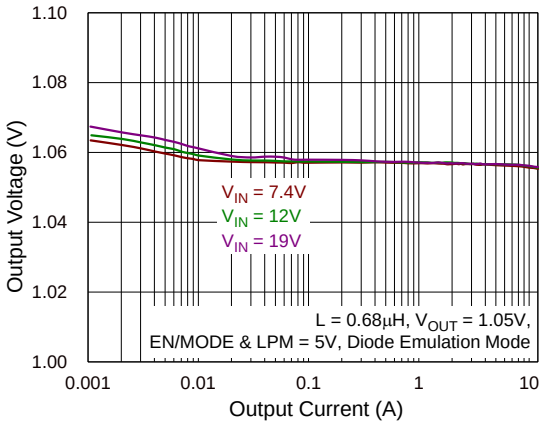
Efficiency vs. Output Current



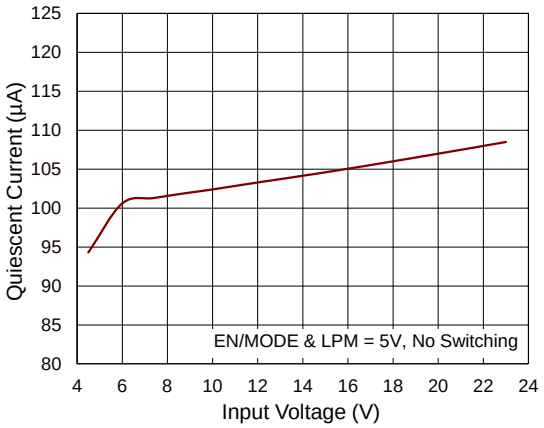
Switching Frequency vs. Output Current



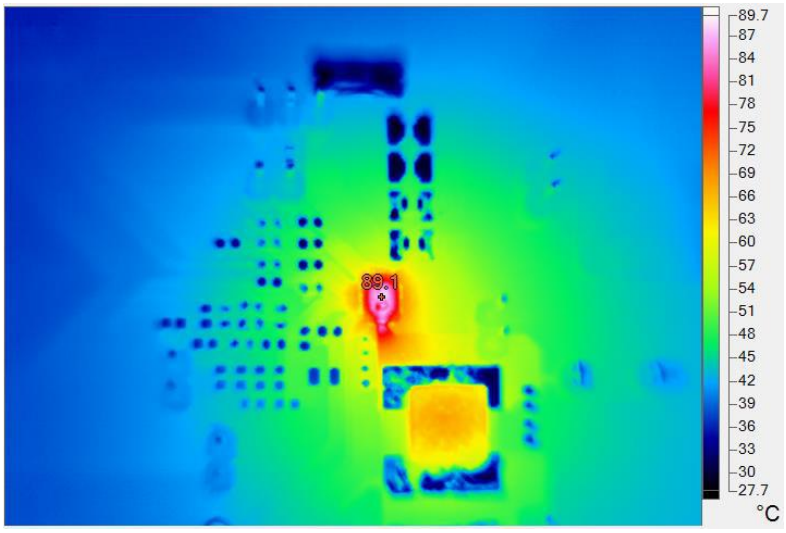
Output Voltage vs. Output Current



Quiescent Current vs. Input Voltage



Thermal Image at V_{IN} = 19V, V_{OUT} = 1.05V, I_{OUT} = 12A



Note: When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the output voltage ripple by touching the probe tip directly across the output capacitor.

Evaluation Board Layout

Figure 1 to Figure 4 are RT6321AN-A Evaluation Board layout. This board size is 89mmx76mm and is constructed on four-layer PCB, outer layers with 2 oz. Cu and inner layers with 1 oz. Cu.

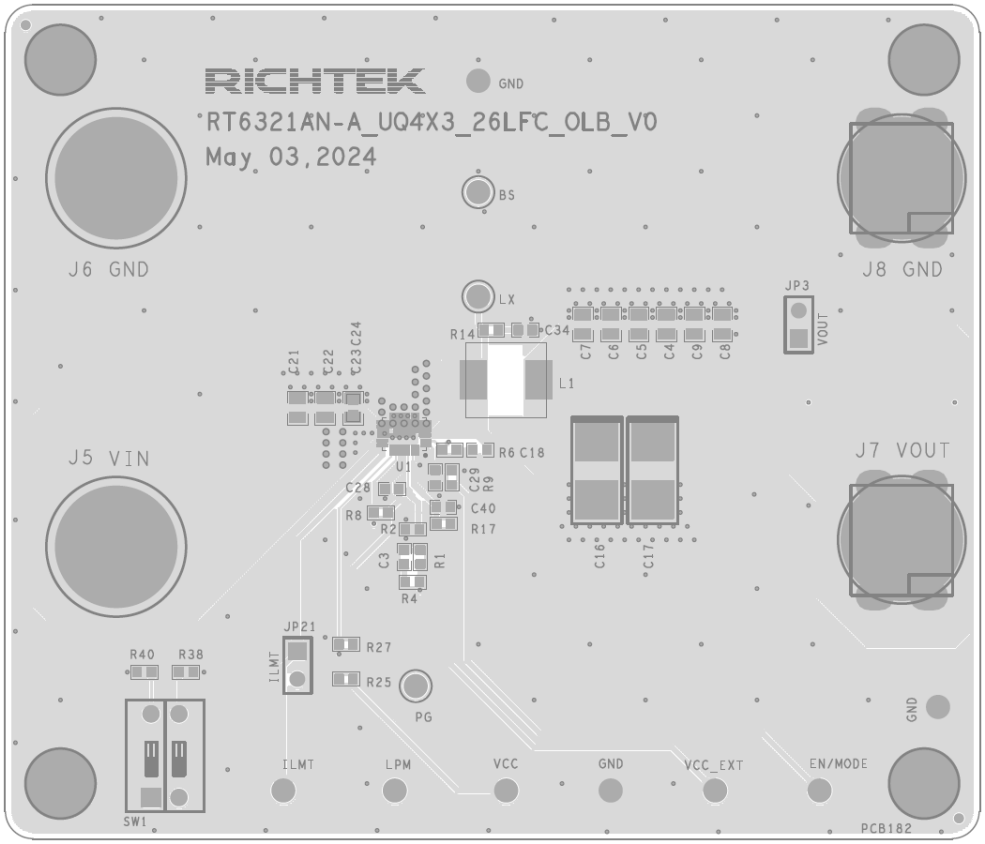


Figure 1. Top View (1st layer)

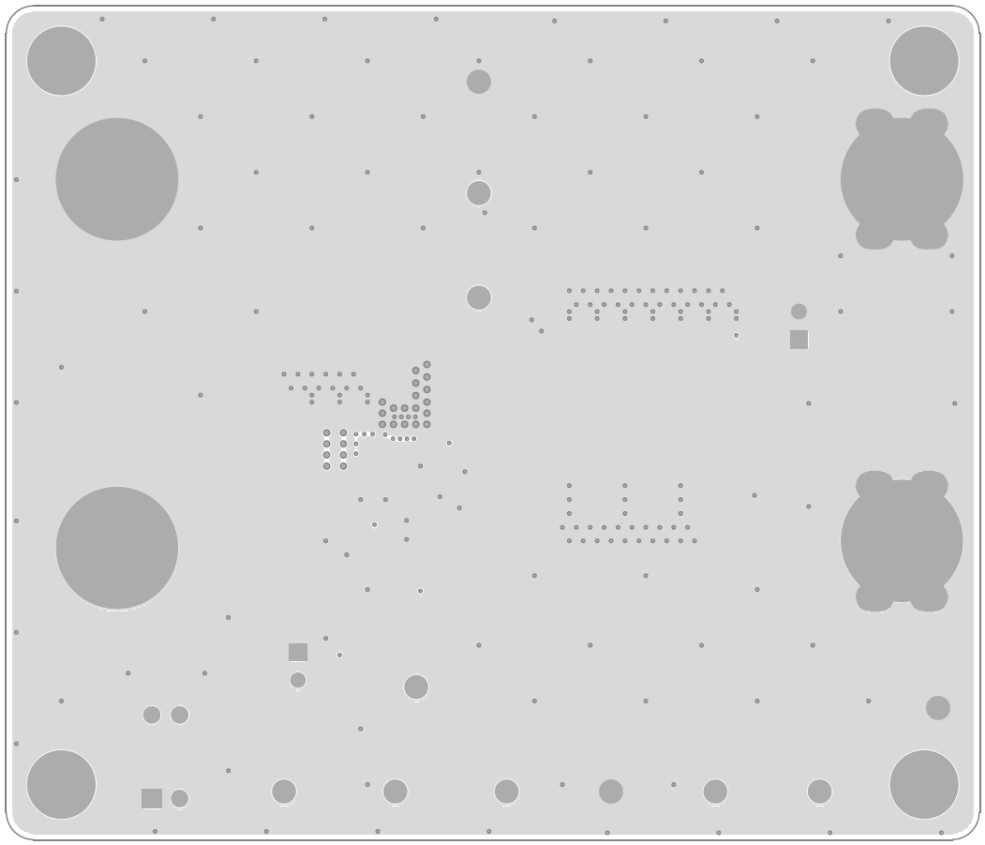


Figure 2. PCB Layout—Inner Side (2nd Layer)

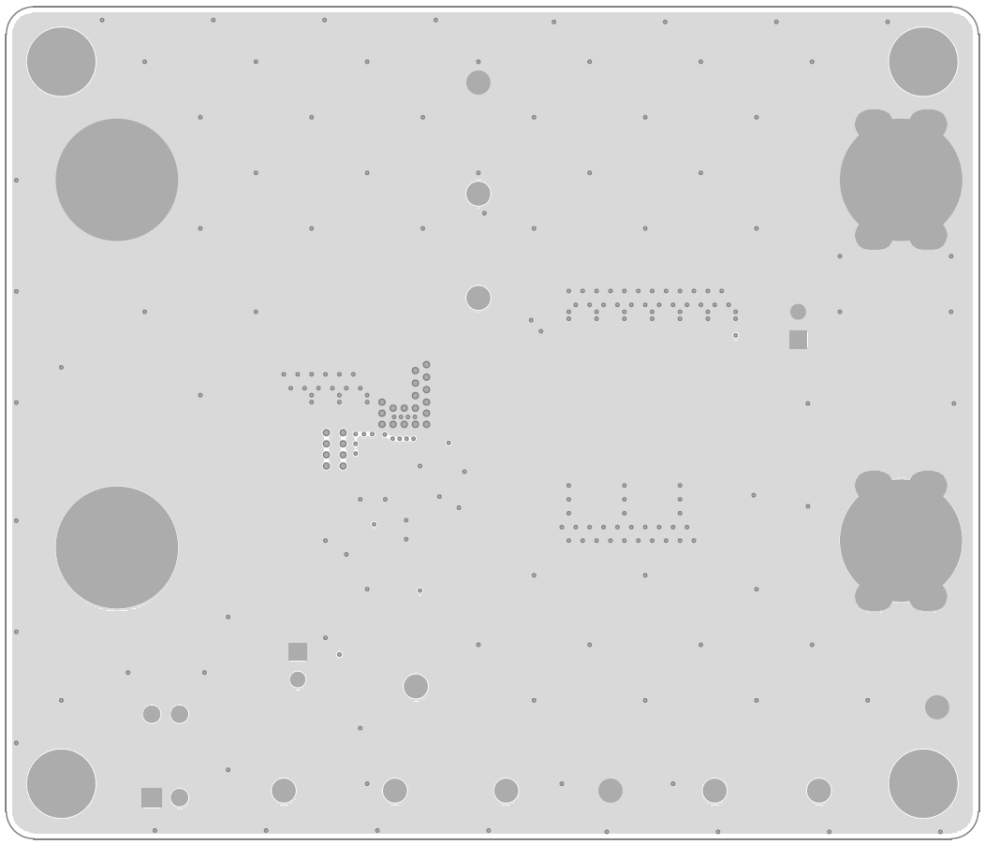


Figure 3. PCB Layout—Inner Side (3rd Layer)

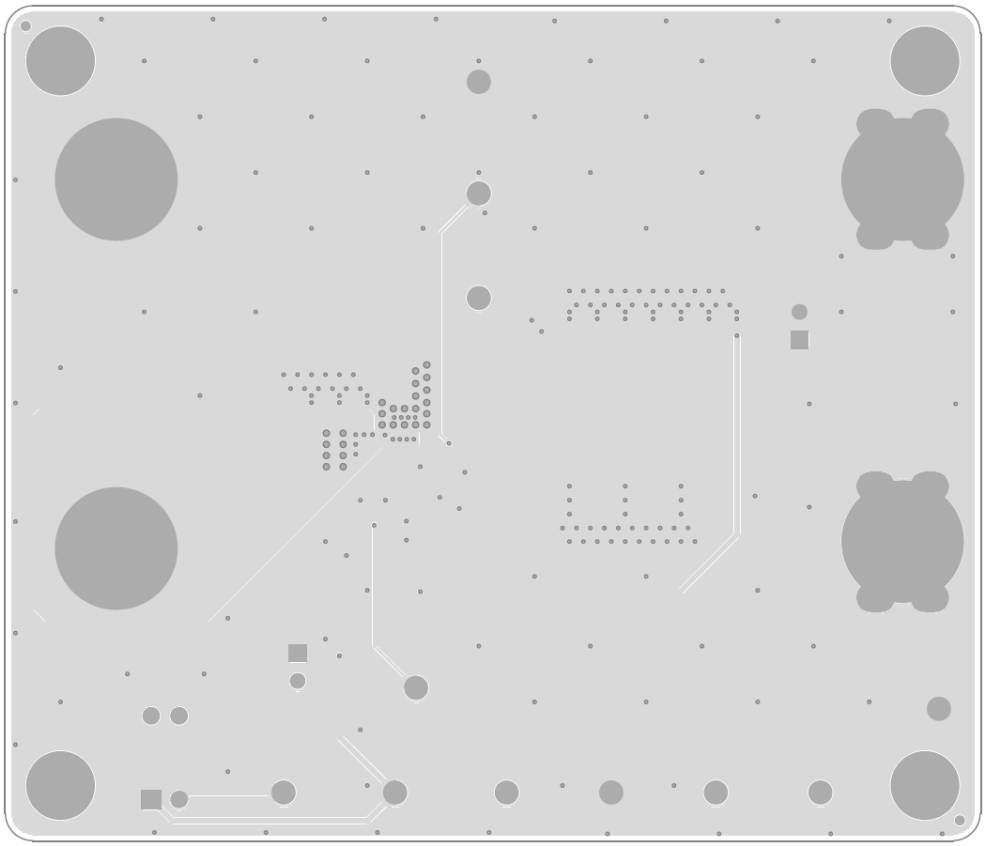


Figure 4. Bottom View (4th Layer)

More Information

For more information, please find the related datasheet or application notes from Richtek website http://www.richtek.com.

Important Notice for Richtek Evaluation Board